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(54) Title: PRECISE MOS IMAGER TRANSFER FUNCTION CONTROL FOR EXPANDED DYNAMIC RANGE IMAGING
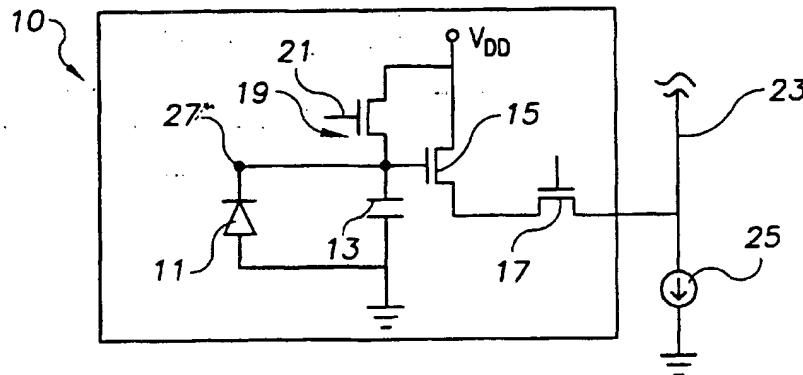
(57) Abstract: There is provided an imaging system including a MOS pixel array having a number, r, of rows of pixels. Each pixel of the array includes a light detecting element, a reset node connected to the light detecting element for controlling dissipation of photogenerated charge produced by the light detecting element, and a sense node connected to the light detecting element for measuring photogenerated charge produced by the light detecting element. A charge control voltage generation circuit is provided, having topology for producing a plurality of charge control voltages selected to control dissipation of photogenerated charge produced by the light detecting element, in accordance with a corresponding pixel transfer function. A switch circuit is connected to the voltage generation circuit and to the pixel array to apply voltage produced by the charge control voltage generation circuit to reset nodes of pixels. The application by the switch circuit of each of the charge control voltages to a row of pixel reset nodes is characterized by a voltage application settling time, t_s, that is less than about $1/Nrf$, where N is an integer and f is imager frame rate. This provides the ability to implement a desired transfer function, to expand imager dynamic ranger, in a manner that is immune to capacitances of the imager, by causing the voltage spikes, or glitches, associated with imager row capacitance, to decay substantially completely during the time over which an imager pixel row is accessed to apply a control voltage.

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PRECISE MOS IMAGER TRANSFER FUNCTION CONTROL
FOR EXPANDED DYNAMIC RANGE IMAGING

5   This application claims the benefit of U.S. Provisional Application

No. 60/221,856, filed July 28, 2000, the entirety of which is hereby

incorporated by reference.

BACKGROUND OF THE INVENTION

This invention relates to MOS imagers, and more particularly relates

10   to techniques for increasing the dynamic range of a MOS imager.

Conventionally, MOS imagers are characterized by a linear voltage-

to-light response, or transfer function; that is, the imager output voltage is

approximately linearly related to light incident on the imager. Specifically,

the output voltage transfer function is linearly proportional to the intensity

15   of the light incident on the imager. This linear transfer function can be

characterized by a dynamic range, given as the ratio of the highest

detectable illumination intensity of the imager to the lowest detectable

illumination intensity of the imager. It is well understood that the dynamic

range of the transfer function sets the overall dynamic range of the imager.

20   If the dynamic range of a scene exceeds the dynamic range of an imager,

portions of the scene will saturate the imager and appear either completely

black or completely white. This can be problematic for imaging large

dynamic range scenes, such as outdoor scenes.

Conventionally, a MOS imager pixel includes a phototransistor or

25   photodiode as a light detecting element. In operation, e.g., the pixel

photodiode is first reset with a reset voltage that places an electronic charge

across the capacitance associated with the diode. Electronic charge

produced by the photodiode when exposed to illumination then causes

charge of the diode capacitance to dissipate in proportion to the incident

30   illumination intensity. At the end of an exposure period, the change in

diode capacitance charge is detected and the photodiode is reset. The

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amount of light detected by the photodiode is computed as the difference between the reset voltage and the voltage corresponding to the final capacitance charge. The illumination intensity that causes the photodiode capacitance charge to be completely dissipated prior to the end of the

5   exposure period, thereby saturating the pixel, sets the upper end of the pixel dynamic range, while thermally generated photodiode charge and other noise factors set the lower end of the pixel dynamic range.

        A variety of techniques have been proposed for expanding the dynamic range of a MOS imager. In one particularly effective technique,

10   the voltage-to-light transfer function of the imager is modified to be a nonlinear function of illumination intensity, with transfer function slope increasing linearly as a function of illumination intensity. This transfer function modification is typically implemented as a photodiode capacitance charge control function within a CMOS imager pixel.

15   Specifically, in this technique, over the course of an exposure period a control voltage is applied to the photodiode capacitance to control charge dissipation from the capacitance. The charge control voltage is typically decreased from the starting pixel reset voltage value to, e.g., electrical ground, with each control voltage value at a given time during the exposure

20   period setting the maximum charge dissipation of the photodiode. This control voltage decrease acts to increase the photodiode charge dissipation capability, whereby the pixel can accommodate a higher illumination intensity before saturating, and the dynamic range of the pixel is thusly increased. This charge dissipation control overrides the conventional linear

25   voltage-to-charge transfer function of the pixel to produce a nonlinear transfer function, generally referred to as a compressed transfer function, and a correspondingly expanded dynamic range of the pixel and the imager.

        Theoretically, the charge dissipation control voltage applied to a pixel photodiode is preferably continuously adjusted over the course of an

30   exposure period. This enables the production of almost any desired transfer

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function compression characteristic. For many applications, this theoretical condition is not practical, however. Conventional MOS imagers include an array of pixel columns and rows and typically do not include pixel memory. Therefore, at the end of an exposure period each row of pixel values must be

5   immediately read out. But in general, only one row of pixel values can be read out at a time. To accommodate this condition, the exposure periods of the pixel rows are typically staggered in a time sequence corresponding to the sequential pixel row read out. As a result, the desired pixel charge control voltage waveform must also be applied to the pixel rows in a

10   staggered sequence; the same control voltage waveform is applied to every pixel row but is staggered in time between rows.

       As a practical matter, given, e.g., a conventional VGA imager including 480 pixel rows, it would be difficult to deliver 480 continuous-time control voltage waveforms to the imager array or to generate 480 delayed

15   versions of a single continuous-time waveform. It has been found that the approximation of a continuous-time control voltage waveform by a discrete-time, or stepped, control voltage waveform addresses this timing concern while enabling more flexibility and ease in control voltage generation and sequential delivery to a pixel array. In this technique, a desired continuous-

20   time control voltage waveform, or transfer function compression curve, is approximated by voltage steps. This results in a finite number, e.g., eight, of distinct control voltage levels to be applied in a discrete manner to a pixel over the course of that pixel's exposure period. Conventionally, the prescribed discrete-time analog control voltages are generated off-chip from

25   the imager array and then delivered to each pixel row on-chip in a staggered sequence controlled by, e.g., a digital controller. It has been found that this scenario enables good pixel control as well as timing control and additionally provides the ability to modify the transfer function compression characteristic.

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It has been recognized that the discrete analog voltages produced to impose imager transfer function control preferably are regulated to be precise and noise free, and preferably are maintained free of glitches, where a "glitch" is here defined as a rapid excursion, or spike, in the voltage.

5　Without such regulation, the desired compression function could be distorted, with the resulting images including noise or appearing unnatural. Regulation of the control voltages is particularly important as the voltages are switched from one pixel row to the next. Specifically, when a given control voltage is applied from one pixel row to the next, a voltage excursion,

10　or glitch, is produced due to an inherent row switching capacitance. Such an excursion in a voltage source could cause rows of pixels already connected to that voltage to dissipate charge or accumulate charge in a manner not consistent with the desired transfer function.

For this reason, conventional imager configurations typically employ

15　external, off-chip analog control voltage sources having output voltages that are bypassed by large and external bypass capacitors. The bypass capacitors are employed to eliminate glitches due to row switching capacitance as the charge control voltages are sequentially applied to rows of an imager. It has been understood that without the use of such bypass

20　capacitors, a staggered-row control voltage application scenario does meet most imager performance requirements.

The typical row capacitance of a VGA imager is on the order of about 5 pF. In order to effectively reduce switching glitches from this row capacitance by an order of magnitude or more, bypass capacitors for each

25　analog control voltage source are required to each be at least about 50 pF, and more typically are provided as an external capacitor or about 0.1 µF for each external analog voltage generation circuit. This external control voltage generation circuit configuration adds to imager system power consumption, complexity, cost, and overall imager system extent, and

30　influences other imager performance factors. But practical implementation

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of a compressive MOS imager transfer function characteristic has heretofore required accommodation of the bypass capacitor configuration and the limitations imposed by this configuration.

SUMMARY OF THE INVENTION

5   The invention provides the ability to effectively and precisely implement a desired imager and pixel transfer function, to expand imager dynamic range, in a manner that is immune to capacitances of the imager. This is accomplished in accordance with the invention with an imaging system including a MOS pixel array having a number, r, of rows of pixels.

10   Each pixel of the array includes a light detecting element, a reset node connected to the light detecting element for controlling dissipation of photogenerated charge produced by the light detecting element, and a sense node connected to the light detecting element for measuring photogenerated charge produced by the light detecting element. A charge control voltage

15   generation circuit is provided, the circuit having a topology for producing a plurality of charge control voltages selected to control dissipation of photogenerated charge produced by the light detecting element, in accordance with a corresponding pixel transfer function. A switch circuit is connected to the voltage generation circuit and connected to the pixel array

20   to apply voltages produced by the charge control voltage generation circuit to reset nodes of pixels. The application by the switch circuit of each of the charge control voltages to a row of pixel reset nodes is characterized by a voltage application settling time, t_s, that is less than about $1/Nrf$, where N is an integer and f is imager frame rate.

25   This configuration causes the voltage spikes, or glitches, associated with the imager row capacitance, to decay substantially completely during the time over which an imager pixel row is accessed to apply a control voltage. As a result, the voltage spikes have no impact when a sequence of control voltages is applied to rows of an imager, e.g., when the switch circuit

30   is configured to apply the voltages through the imager pixel rows

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sequentially. No bypass capacitors are therefore required, and the charge control voltage generation circuit can be fabricated quite compactly, preferably monolithically with the imager pixel array and switching circuit, e.g., in a CMOS fabrication process. Here all of the voltage generation and

5   switch circuit elements can be fabricated in-line with the imager, e.g., with the switch circuit provided as MOS transistor switches.

In accordance with the invention, for applications in which charge control voltage application to pixel reset nodes is to be carried out across an imager array simultaneously, rather than row-by-row, the voltage spikes, or

10 glitches, associated with the control voltages can be caused to decay substantially completely without impacting imager performance by requiring that the voltage application settling time, t_s, be less than about the duration specified for each of the control voltages in the plurality of control voltages.

15 The invention provides for embodiments in which the light detecting element of MOS imager pixels can be provided as, e.g., a photodiode, a phototransistor, or other suitable configuration. The reset node of the imager pixels can be provided as a MOS reset transistor. The sense node of the imager pixels is preferably connected to the light detecting element at a

20 node corresponding to capacitance of the light detecting element.

In accordance with the invention, the charge control voltage application settling time, t_s, can be specified as $t_s=R_{th}C$, where R_{th} is a Thevenin resistance of the charge control voltage generation circuit topology and C is an effective capacitance of the pixel array. To meet the

25 requirement of the invention for causing voltage spikes to decay sufficiently rapidly, the Thevenin resistance, R_{th}, of the charge control voltage generation circuit topology, is preferably less than $1/NrfC$, where $N \geq 2$.

The invention provides embodiments wherein the charge control voltage generation circuit topology includes a plurality of resistors, which in

30 one preferable example are connected in series between two voltages. The

resistors can be provided as monolithically fabricated polysilicon resistors for applications in which integration of the entire imager system is preferred. A voltage source and/or a current source can be included with the resistor network, and each can be provided as variable sources; it can be

5   preferred to provide the current source as a transistor current source. In a topology including a series connection of resistors, the series can be connected between, e.g., a power supply voltage and electrical ground. Here a current source can be connected between one of the plurality of resistors and the power supply voltage or electrical ground. In other embodiments,

10   the invention provides for a charge control voltage generation circuit topology that includes a digital register for each charge control voltage in the plurality of voltages, or that includes a sample-and-hold amplifier for each charge control voltage in the plurality of voltages.

It can be preferred for many applications to provide a charge control

15   voltage generation circuit configuration such that at least one of the voltages produced by the circuit is a variable voltage. In one embodiment, each of the charge control voltages is a substantially constant voltage level. The plurality of voltages here produce a stepped sequence of voltage levels. Alternatively, the plurality of charge control voltages can together produce a

20   substantially continuously-changing voltage level. For MOS photodiode-based imagers, it can be preferred to provide a stepped sequence of decreasing control voltage levels to increase the dynamic range of the imager. Imager dynamic range can particularly be increased by selecting the plurality of control voltage levels to impose a nonlinear transfer function

25   on the imager pixels.

The imager system of the invention and the corresponding charge control voltage generation and application techniques enable a very efficient and elegantly non-complex imager system design and operation. By eliminating the need for large bypass capacitors, the system of the invention

30   can be compactly fabricated, e.g., as a single monolithically-integrated

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system. This high degree of integration enables the use of the imaging

system in a wide range of consumer and specialty photography,

surveillance, robotic control, and other applications for which high

performance, low cost, efficiency, and size are all preferred.

BRIEF DESCRIPTION OF THE DRAWINGS

5

Fig. 1 is a schematic diagram of a pixel provided in accordance with

the invention for enabling expanded imager dynamic range;

Fig. 2 is a plot of an example discrete-time charge control voltage

profile, as a function of time, as provided by the invention;

10

Fig. 3 is a plot of a pixel photodiode energy barrier profile produced

by the voltage profile plotted in Fig. 2;

Fig. 4 is a plot of a pixel photodiode capacitance charge-to-

illumination intensity function produced by the voltage profile plotted in

Fig. 2;

15

Fig. 5 is a reproduction of the voltage profile plot of Fig. 2, here also

illustrating voltage spikes present in the voltage profile and the

requirement of the invention that the voltage spikes remain below the

highest illumination intensity not to be compressed by a given charge

control voltage level;

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Figs. 6A, 6B, and 6C are example resistor circuit implementations

provided by the invention for producing charge control voltage levels in

accordance with the invention;

Fig. 7 is a first example resistor circuit implementation including a

current source in accordance with the invention for producing charge control

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voltage levels in accordance with the invention;

Fig. 8 is an example implementation of the current source of Fig. 7 in

accordance with the invention;

Fig. 9 is a second example resistor circuit implementation including a

current source in accordance with the invention for producing charge control

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voltage levels in accordance with the invention;

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Fig. 10 is an example resistor circuit implementation including a voltage source in accordance with the invention for producing charge control voltage levels in accordance with the invention; and

Figs. 11 and 12 are example mixed digital and analog circuit
5   implementations provided by the invention for producing charge control voltage levels in accordance with the invention by employing a digital register for each control voltage and a sample-and-hold amplifier for each voltage, respectively.

DETAILED DESCRIPTION OF THE INVENTION

10   Referring to Fig. 1, the operation of a pixel 10 provided by the invention for enabling expanded dynamic range by application of stepped charge control voltages is described, Fig. 1 providing a schematic diagram of the pixel. This example pixel configuration employs a photodiode, but it is to be recognized that in general, the pixel can include other light collecting
15   configurations, embodied as, e.g., a phototransistor, a photogate, or other selected configuration. In the current example, a photodiode 11 of the pixel produces a current of photogenerated electrical charge in response to light incident on the pixel. The resulting photocurrent is directed to a charge-sensing capacitor 13. The charge-sensing capacitor 13 is in practice
20   provided as a collection of parasitic capacitances that are associated with a charge sense node 27 of the photodiode.

A MOS transistor 15 operates as a source follower that buffers the voltage on the capacitor 13 nondestructively to a column line 23 for read out of the voltage. Specifically, a row select MOS switch 17 activates the source
25   follower transistor 15 when the particular row is selected to thereby enable the capacitor voltage measurement. When the row select MOS switch 17 of the row is turned on, and a current source 25 is connected to the source of the MOS transistor 15, the MOS transistor 15 and the current source 25 operate as a source-follower configuration to buffer the voltage on the
30   photodiode capacitor 13 to the column line 23 for determining the capacitor

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voltage at the end of an exposure period, to in effect measure the

photogenerated charge.

     Referring also to Fig. 2, a stepped, i.e., discrete-time, charge control

voltage profile, $V(t)$, is applied to the gate 21 of a reset transistor 19 of the

5   pixel over the course of an exposure period for control of the charge

dissipation from the photodiode capacitance. The gate 21 of the reset

transistor 19 thereby operates as a reset node for delivering charge control

voltages to the pixel photodiode. While this reset node is shown in this

example as a MOS transistor gate, it is to be recognized that other reset

10   node configurations can be accommodated by the control technique of the

invention. For clarity of discussion, in the plot of Fig. 2 only three different

control voltage step values, V_1, V_2, V_3, are shown along with the pixel reset

voltage, V_{RESET}, but it is to be recognized that additional voltage levels can be

provided as prescribed by a desired transfer function compression

15   characteristic.

    Fig. 3 is a plot of the pixel photodiode charge dissipation energy

barrier, $b(t)$, as a function of time, that is produced by the charge control

voltage profile of Fig. 2. Fig. 4 is a plot of the resulting charge-to-

illumination intensity transfer function, or compression curve, that is

20   produced by the charge control, here for a charge profile, $Q(I)$ produced by a

number, n, of illumination intensity levels, I. It is to be recognized that

although the photodiode energy barrier profile, $b(t)$, and charge compression

curve, $Q(I)$, are here plotted for clarity as increasing functions, in operation

the photodiode capacitance voltage decreases over the course of an exposure

25   period in the manner described above.

    It can be seen from the plots of Figs. 2, 3, and 4 that the discrete

changes in photodiode energy barrier height produced by stepped charge

control voltage as function of time give rise to a corresponding piecewise

linear transfer function between the incident light intensity and the charge

30   of the photodiode capacitor. The number of steps in the applied voltage

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profile and energy barrier height function thereby correspond directly to the number of piecewise linear sections in the charge-to-illumination intensity transfer function.

A typical CMOS imaging array in which the pixel of the invention can
5   be implemented consists of pixel rows and columns; e.g., in a VGA CMOS imager, the pixels are arranged in a 640x480 array having 640 pixels in a row and 480 rows. The gates of reset transistors from the 640 pixels in each row can be provided as connected together at a point where the charge control voltage waveform is to be applied, whereby the waveform can be
10.   applied simultaneously to all pixels in a given row. The stepped control voltage waveform profile, like that of Fig. 2, is applied sequentially from the upper-most row to the bottom-most row of the pixel array, or is applied in another selected manner as-prescribed for a given imager operation.

In one scenario, each voltage is applied to successive pixel rows with
15   a voltage application delay between rows equal to the frame period, divided by the number of rows. This sequential voltage application can be carried out, e.g., by a bank of switches, implemented as, e.g., MOS transistors, which connect the rows to appropriate charge control voltages in the manner described in detail below.

20   Employing conventional charge control voltage generation circuitry, it has been found that without large external bypass capacitors, spikes in the control voltage can occur as the voltage is applied from one pixel row to the next. The total capacitance per row presented to the voltage generation circuit is typically on the order of about 5 pF. As each pixel row is switched
25   from one voltage step to another, the 5 pF row capacitance is also switched to a different voltage source. It is this capacitance switching that causes voltage spikes, or "glitches," in the applied control voltage if the voltage sources are not bypassed by large capacitors. As explained above, the positive voltage spikes are destructive because they prevent the pixel
30   voltage from decreasing in response to the incident light, and thereby

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disallow the pixel from following the prescribed charge-to-illumination intensity transfer function.

Referring to Fig. 5, the control voltage profile plot of Fig. 2 is reproduced, here shown with voltage spikes 25 that are produced by pixel
5 row switching capacitance. In the steady-state, the charge control voltage waveform profile exhibits voltage spikes 25 like that shown in the plot of Fig. 5. The voltage spikes are positive and of a magnitude that is determined by the number of pixel rows and the charge control voltage waveform profile. A sequence 27 of spikes is applied to each row as the rows
10 are sequentially addressed, with each spike separated in time by the row access duration.

In accordance with the invention, a pixel charge control voltage generation circuit is provided that renders such voltage spikes, or glitches, harmless. Referring to Fig. 5, in accordance with the invention, the voltage
15 generation circuit produces a waveform whereby any voltage spikes present at a given voltage level remain below a pixel voltage waveform value 30 that corresponds to the highest light intensity not to be compressed in that voltage step segment of the control voltage profile, in the manner shown in Fig. 5. In Fig. 5, example voltage spikes that have been controlled to meet
20 this requirement by falling below pixel voltage waveform levels are shown, with the tangential lines 30 drawn from one edge of a voltage step segment to the next edge of a voltage step segment indicate the highest light intensity not to be compressed during that segment. This control technique disables a scenario wherein the pixel voltage waveform would be pulled up
25 by the voltage spikes to result in incorrect photodiode charge dissipation. Any illumination intensity higher than that not to be compressed is automatically clamped by control voltages, whereby the voltage spikes have virtually no effect on compressed or uncompressed illumination intensities.

More specifically, as shown in Fig. 5, it is recognized in accordance
30 with the invention that the temporal spacing between voltage spikes in

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steady state corresponds to the pixel row access time, t_{ROW}, and therefore, by controlling voltage spikes to substantially completely decay during this row access time, a voltage spike will have no impact as voltages are switched between rows. This control is imposed in the invention by controlling the

5   resistor-capacitor (RC) time constant, or correspondingly, the settling time, t_s, of the charge control voltage application. Specifically, the RC time constant, or settling time, of the of charge control voltage application to a given pixel row is required by the invention to be less than, and preferably much less than, the pixel row access time, as:

10                                 $$t_s = R_{th}C < t_{ROW}   \qquad (1)$$

where R_{th} is the effective Thevenin resistance of the voltage generation circuit and C is the total capacitance of the entire pixel array that is presented to the control voltage.

As explained above, typically the pixel row access time is determined

15   by the imager frame rate. The requirement of the invention for rendering the imager immune to voltage spikes can therefore be stated as:

$$t_s = R_{th}C < \frac{1}{rf}   \qquad (2)$$

where r is the number of rows of the imager array and f is the imager frame rate being employed.

20   As an example of this technique, consider an imager frame rate of 30 frames/second employed with a VGA imager, having 480 rows. This scenario produces a pixel row access time of about 69 μs. The capacitance of such an imager is on the order of 5 pf x 480 rows=2.4 nF for a 480 row VGA imager characterized by a 5 pF row switching capacitance. For this case, to

25   meet the requirements of the invention as specified by Expressions (1) and (2) above, the effective Thevenin resistance of the charge control voltage generation circuit is preferably maintained no larger than 65 μs/2.4 nF=27 kΩ, and preferably is at least about 2-5 times less than this value, such that

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voltage spikes are controlled to decay faster than the pixel row access time and therefore be rendered harmless.

In accordance with the invention, this voltage application control can be adapted to the particular technique employed in a given imager for

5   addressing each pixel row. The examples discussed above were directed to a row address technique in which each row is addressed separately in sequence, thereby requiring a staggered delivery of control voltages through the rows of an imager. In a further example, all pixel imager rows are addressed simultaneously, thereby eliminating a requirement for sequential

10   pixel row addressing.

In this example, in order to control voltage spikes to decay sufficiently quickly to be rendered harmless, the invention requires that the settling time, t_s, of the simultaneous control voltage application to all of the pixel rows be less than the duration, t_v, for each of the n control voltages in the

15   sequence of control voltages. In other words, the setting time of the charge control voltage application is given as:

$$t_s = R_{th}C < t_v, \tag{3}$$

for each of the 1 to n voltages, V, employed in the selected transfer function control. Referring back to the plot of Fig. 2, the duration, t_v, of each of the

20   control voltages corresponds to the length of time during which the transfer function, $V(t)$, is held at a given voltage level.

It is recognized that to implement this control technique as a practical matter, stepped, i.e., discrete-time, control voltages are to be employed. The use of continuous time, i.e., constantly changing, analog

25   voltages would not be practical. However, the voltage control technique described previously, for use with sequential voltage application through rows of an imager, is not limited to the use of discrete-time voltages; continuous analog voltages can be there employed. For many applications, discrete-time voltages sufficiently approximate continuous-time voltages

30   and can be more easily generated, and therefore are often preferred.

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With the conditions of either of expressions (2) or (3) above met, no bypass capacitors are required of the voltage generation circuitry, and no particular care need be taken in the sequential or simultaneous pixel row access to inhibit voltage spikes; instead, in accordance with the invention,

5   the charge control voltage application is carried out in a manner that is immune to the voltage spikes. This results in reduction in imager complexity and cost, and enables a particularly advantageous configuration in which the charge control voltage generation circuitry can be monolithically integrated on-chip with the imager array itself, in the

10   manner described in detail below.

A first example embodiment of a charge control generation circuit provided by the invention, which can be configured to produce a number, n, of barrier voltages $V_1, V_2, ..., V_n$, is schematically shown in Fig. 6A. A number, $n+1$, of resistors are connected in series between two voltages V_{TOP}

15   and V_{BOTTOM}. An output voltage tap is provided at selected locations in the resistor topology, e.g., between each of the resistors, to produce n tap voltages $V_1, V_2, ..., V_n$, corresponding to n charge control voltages to be supplied to each pixel to form a discrete-time charge control profile over the duration of the imager exposure period. Each of the n control voltages is

20   then given as:

$$V_1 = V_{TOP} - \frac{R_1}{R_{TOTAL}}(V_{TOP} - V_{BOTTOM})$$

$$V_2 = V_1 - \frac{R_2}{R_{TOTAL}}(V_{TOP} - V_{BOTTOM})$$

$$\hspace{10cm} (4)$$

$$V_n = V_{n-1} - \frac{R_n}{R_{TOTAL}}(V_{TOP} - V_{BOTTOM})$$

where $R_{TOTAL} = R_1 + R_2 + \cdots + R_{n+1}$

The worst-case Thevenin resistance, R_{th} of this circuit is found to be $\frac{R_{TOTAL}}{4}$.

In order to remove the effect of voltage spikes in accordance with the

invention, $R_{th} = \dfrac{R_{TOTAL}}{4}$ is therefore required to be implemented as a value

below the imager row capacitance divided by pixel access row time. As stated above, in a typical VGA imager, this value corresponds to a Thevenin resistance of about 27 kΩ. Thus, in accordance with the invention,

5    $\dfrac{R_{TOTAL}}{4}$ should be no larger than about 27 kΩ and preferably is at least about

2-5 times less than this value such that the glitches decay faster than the pixel access row time.

Preferably, V_{TOP} corresponds to the reset voltage V_{RESET}. In order to provide the greatest signal range for the pixel, V_{TOP} preferably is kept as

10   high as possible, e.g., close to the positive power supply voltage V_{DD}, or can even be implemented as a voltage source higher than V_{DD} if a dc-dc converter is employed. It is also preferred that the charge control voltages generated preferably be quiet and stable, requiring both V_{TOP} and V_{BOTTOM} to be quiet and stable. Most imagers have two sets of power supply voltages; one set for

15   analog functions and the other set for digital functions. In such imagers, analog V_{DD} (AVDD) and analog ground (AGND) are quieter, and hence are preferred as sources for supplying the voltages V_{TOP} and the V_{BOTTOM}, respectively. Alternatively, the voltage V_{TOP} can be produced by stable voltage sources such as a bandgap voltage source or a Zener diode whose

20   voltages are referenced to AGND. This embodiment renders V_{TOP} and all produced charge control voltages independent of variations in AVDD. The drawback with this approach, however, is that the voltage V_{TOP} must be lower than AVDD. A low-dropout type regulated voltage source can be employed to alleviate this drawback.

25   In accordance with the invention, the voltages produced by the voltage generation circuit, e.g., the circuit of Fig. 6A, are delivered to each pixel row of an imager array in sequence, following the pixel row access time requirements defined above. In one advantageous implementation, a digital shift register is employed to connect each pixel row to one of the analog

control voltage levels. For example, an eight-bit digital shift register can be employed for controlling connection of a pixel row to one of eight analog charge control voltage levels. Preferably the row switch for making such connection is provided as a MOS transistor. A digital control rule is

5   preferably implemented for connecting each pixel row to one of the generated voltage levels at a given time during the exposure period. As the shift register is advanced, the control voltages are applied to sequential pixel rows. A digital clock generator circuit is preferably employed to produce shift register timing control for sequential application of the

10   voltages.

The invention contemplates a wide range of charge control voltage generation circuit configurations beyond that shown in Fig. 6A. Figs. 6B and 6C are schematic drawings of alternative circuit configurations for producing a number of charge control voltage levels in a manner that

15   enables control of the Thevenin resistance of the circuit. No particular circuit element connection topology or output voltage tap topology are required by the invention; rather, the equivalent Thevenin resistance of the circuit must meet the requirements for producing a settling time that is immune to charge control voltage spikes. Fixed-value circuit elements are

20   also not required by the invention; for example, one of the voltage sources, e.g., V_{BOTTOM}, can be provided as an adjustable voltage source for enabling adjustment of the charge control voltages and their resulting compression function.

A preferred example embodiment of the voltage generation circuit of

25   the invention is schematically shown in Fig. 7. In this embodiment, shown for clarity as a series-connection of resistors, the bottom-most resistor R_{n+1} is replaced by a current source, producing a current, I. It is to be recognized that other circuit topologies, such as those shown in Figs. 6B and 6C, can also be employed here. The current source preferably is a transistor current

30   source referenced to a silicon bandgap reference voltage or another stable

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voltage to maintain the current stable against power supply and temperature variations. Alternatively, the current source can be designed to have a non-zero temperature coefficient that cancels the temperature coefficient of the resistors. The charge control voltages produced by this

5   circuit are given as:

$$V_1 = V_{TOP} - IR_1$$
$$V_2 = V_{TOP} - I(R_1 + R_2)$$

(5)

$$V_n = V_{TOP} - I(R_1 + R_2 + \cdots + R_n)$$

The worst-case Thevenin resistance, R_{th}, is in this case found to be

10   $R_{TOTAL} = R_1 + R_2 + \cdots + R_n$. In order to remove the effect of spikes in the charge control voltage application in accordance with the invention, R_{TOTAL} is to be kept below the imager array row switch capacitance divided by pixel row access time. As stated above, in a typical VGA imager, this value corresponds to about 27 kΩ. Thus, R_{TOTAL} should be no larger than about 27

15   kΩ, and preferably is maintained about 2-5 times less than this value for such an imager for controlling glitches to decay faster than the row time.

The advantage of this circuit embodiment of the invention is that any variation in V_{TOP} causes the same variation to be produced in each of the charge control voltages. As a result, the differences between the reset

20   voltage and control voltages are maintained constant regardless of variations in the voltage V_{TOP}. Typically, imager read-out circuitry employs a double sampling technique that subtracts the reset level from the measured output signal. This technique cancels the effect of the reset level changes due to any variation in the voltage V_{TOP}. In addition, with

25   differences between the reset voltage and charge control voltages maintained constant, double sampling cancels the effect of charge control voltage variations caused by V_{TOP} variations, as given in Expression (5).

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Therefore, the voltage V_{TOP} can be directly connected to the positive power supply V_{DD}, reducing the complexity of the system considerably.

Another advantage of this embodiment is that the voltage levels produced by the circuit, and the corresponding compression function, can be 5   easily adjusted by varying the current, I, following the rules of expression (5) above for producing voltages based on resistor values and the level of current. This adjustment of current can be carried out by the imager user in real time, e.g., as conditions of a scene change in a manner that makes adjustment of the imager transfer function desirable. An ability to change 10   the imager transfer function on-the-fly can be particularly important for imager applications in which the dynamic range of the scene can change quickly. A circuit topology that includes a current source, as in the example circuit of Fig. 7, can therefore be preferred for many applications.

An example embodiment of the current source employed in the circuit 15   of Fig. 7 is schematically shown in Fig. 8. The voltage V_{REF} is preferably provided by a silicon bandgap reference voltage or a Zener diode voltage. An operational amplifier 31, and a MOSFET 32 constitute a unity-gain negative feedback loop whereby the voltage across a resistor 33 is maintained at the voltage V_{REF}. Because the drain current of the MOSFET 20   32 is equal to its source current, the output current, I, of the current source is given as:

$$I = \frac{V_{REF}}{R} \tag{6}$$

25   The resistor R is preferably fabricated as the same type of resistor configuration as $R_1, R_2, \ldots R_n$ of the voltage generation circuit so that the spacing between the barrier voltages depends only on matching between these resistors independent of temperature coefficient of the resistors, given that the temperature coefficients of the resistors cancel out. The output

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current I, of the current source can be varied by varying the voltage V_{REF} if the adjustment of the compression function is desired.

A further example embodiment of a control voltage generation circuit provided by the invention is schematically shown in Fig. 9. This example illustrates that a current source can be configured at the "top" of the circuit, adjacent to the top voltage source, here the power supply, V_{DD}, with the bottom voltage source here provided as electrical ground. The advantage of this embodiment is that the current source effectively isolates noise in the power supply voltage and the charge control voltages are referenced to the quieter ground node. The disadvantage here is that the voltage at the top of the resistor network is required to be lower than the power supply voltage, V_{DD}, to produce a voltage drop across the current source that is sufficient for its functionality. But using a PMOS transistor, this voltage drop can be reduced to below about 200 mV, which is typically small enough to not significantly affect the signal range.

A further example embodiment of the charge control voltage generation circuit of the invention is schematically shown in Fig. 10. In this embodiment a voltage source, V_S, is referenced to the power supply voltage, V_{DD}, as the bottom voltage source, V_{BOTTOM}, while the power supply voltage, V_{DD}, is itself employed as the top voltage, V_{TOP}. Such a voltage source can be provided as, e.g., a band-gap reference based voltage source or a Zener diode.

In a further example charge control voltage generation circuit embodiment shown schematically in Fig. 11, digital-to-analog converters (DAC's) are employed to generate the charge control voltages. In this embodiment, a number, n, of DACs 50 are employed to generate n independent control voltage levels. The prescribed voltage levels are programmed by storing the corresponding digital voltage value in digital registers 54 for the DACs. A given digital register to which a voltage value is to be written is enabled by the *enable* signal. Once the voltage value is

stored in a register, the output of the corresponding DAC is set at the corresponding voltage determined by the data in the register. Although more complicated than other embodiments, this embodiment allows more flexibility in setting an charge-to-illumination intensity compression

5   function because the DAC's can be programmed to produce different charge control voltages.

In a further circuit embodiment provided by the invention, shown schematically in Fig. 12, a single DAC 60 is employed with a number, n, of sample-and-hold amplifiers (SHAs) 64, corresponding to the number of

10   charge control voltage levels to be produced. The DAC sequentially generates control voltages that are sampled and held in the SHAs as the *hold* signal is sequentially activated for the SHAs. This embodiment provides the capability of individually programming the control voltages without the complexity of multiple DAC's. For any digital embodiment of a

15   control voltage generation circuit, it is preferred, as explained above, that the settling time of the voltage application be less than the pixel row access time such that voltage spikes in the control voltage cannot impact the charge control voltage profile.

Whatever circuit implementation is selected for generating the charge

20   control voltage levels, it is preferred in accordance with the invention that the voltage generation circuit be fabricated monolithically, on-chip with the imager array. The substrate on which the imaging array and voltage generation circuitry are integrated can be provided as a silicon or other semiconductor substrate. Preferably, the substrate is compatible with

25   CMOS fabrication processes, which can be preferred for producing a MOS imager and corresponding electronics. The resistors of the voltage generation circuitry preferably are fabricated as polysilicon resistors, produced by the MOS fabrication process. Monolithic integration of the voltage generation circuit is also advantageous in that such enables efficient

30   monolithic integration of the digital voltage switching control circuitry

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described above. The invention therefore contemplates that for most

applications, monolithic single-chip integration of an imager array with the

voltage generation circuitry and switching circuitry is preferred.

The invention contemplates that monolithic integration of the imager

5   array and voltage generation circuitry can optionally include monolithically-

integrated bypass capacitors, if desired for a particular application, but such

is not required, given the voltage spike control technique of the invention

described above. It is a common practice to utilize unused areas of a chip for

on-chip bypass capacitors for various circuit voltages which are desired to

10   stay quiet. The invention does not inhibit following such conventional

practice to bypass on-chip control voltages with on-chip capacitors. If such

is carried out, however, caution must be exercised. While the addition of the

on-chip bypass capacitors generally reduces the magnitude of glitches, such

capacitors increase the RC time constant of the decay of glitches. Thus, to

15   meet the requirements of the invention, the Thevenin resistance of the

voltage generation circuitry must be made correspondingly smaller,

following the considerations given above.

Fundamentally, as explained above, the invention does not require

bypass capacitors and can most advantageously be employed by eliminating

20   bypass capacitors. The voltage spikes, or glitches, associated with

sequential charge control voltage application to pixel rows of an imager are

controlled to substantially completely decay during the characteristic pixel

array row access time. This control ensures that any glitches appearing in

the control voltage waveforms will have no effect on pixel readout data. In

25   accordance with the invention, this eliminates the need for large bypass

capacitors for removing glitches in the conventional manner, and thereby

enables monolithic integration of the voltage generation circuitry in a

manner that was conventionally understood to not be feasible. It is

recognized, of course, that those skilled in the art may make various

30   modifications and additions to the voltage generation circuitry described

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above without departing from the spirit and scope of the present

contribution to the art. Accordingly, it is to be understood that the

protection sought to be afforded hereby should be deemed to extend to the

subject matter of the claims and all equivalents thereof fairly within the

5   scope of the invention.

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We Claim:

1.   1.   An imaging system comprising:

2   a MOS pixel array having a number, r, of rows of pixels, each pixel

3   including a light detecting element, a reset node connected to the light

4   detecting element for controlling dissipation of photogenerated charge

5   produced by the light detecting element, and a sense node connected to the

6   light detecting element for measuring photogenerated charge produced by

7   the light detecting element;

8   a charge control voltage generation circuit including a circuit topology

9   for producing a plurality of charge control voltages selected to control

10 dissipation of photogenerated charge produced by the light detecting

11 element, in accordance with a corresponding pixel transfer function; and

12   a switch circuit connected to the voltage generation circuit and

13 connected to the pixel array to apply voltages produced by the charge

14 control voltage generation circuit to reset nodes of pixels, application by the

15 switch circuit of each of the charge control voltages to a row of pixel reset

16 nodes being characterized by a voltage application settling time, t_s, that is

17 less than about $1/Nrf$, where N is an integer and f is imager frame rate.

1   2.   The imaging system of claim 1 wherein the charge control

2   voltage generation circuit and the switch circuit are monolithically

3   integrated with the MOS pixel array.

1   3.   The imaging system of claim 1 wherein the pixel array, the

2   charge control voltage generation circuit and the switch circuit are together

3   monolithically fabricated as CMOS.

1   4.   The imaging system of claim 1 wherein the pixel light

2   detecting element comprises a photodiode.

1   5.   The imaging system of claim 1 wherein the pixel light

2   detecting element comprises a phototransistor.

1   6.   The imaging system of claim 1 wherein the reset node

2   comprises a gate of a MOS reset transistor.

1   7.   The imaging system of claim 1 wherein the sense node is

2   connected to the light detecting element at a node corresponding to

3   capacitance of the light detecting element.

1   8.   The imaging system of claim 1 wherein the charge control

2   voltage application settling time, t_s, is given as $t_s=R_{th}C$, where R_{th} is a

3   Thevenin resistance of the charge control voltage generation circuit topology

4   and C is an effective capacitance of the pixel array.

1   9.   The imaging system of claim 8 wherein the Thevenin

2   resistance, R_{th}, of the charge control voltage generation circuit topology, is

3   less than $1/NrfC$, where $N \geq 2$.

1   10.   The imaging system of claim 1 wherein at least one of the

2   voltages produced by the charge control voltage generation circuit comprises

3   a variable voltage.

1   11.   The imaging system of claim 1 wherein the charge control

2   voltage generation circuit topology comprises a plurality of resistors and a

3   voltage source.

1   12.   The imaging system of claim 1 wherein the charge control
2   voltage generation circuit topology comprises a plurality of resistors and a
3   current source.

1   13.   The imaging system of claim 12 wherein the current source
2   comprises a variable current source.

1   14.   The imaging system of claim 12 wherein the current source
2   comprises a transistor current source.

1   15.   The imaging system of claim 1 wherein the charge control
2   voltage generation circuit topology comprises a series connection of a
3   plurality of resistors between two voltages.

1   16.   The imaging system of claim 15 wherein the charge control
2   voltage generation circuit topology resistors comprises monolithically
3   fabricated polysilicon resistors.

1   17.   The imaging system of claim 15 wherein the two voltages of the
2   charge control voltage generation circuit topology comprise a power supply
3   voltage and electrical ground.

1   18.   The imaging system of claim 17 wherein the charge control
2   voltage generation circuit topology further comprises a current source
3   connected between one of the plurality of resistors and electrical ground.

1   19.   The imaging system of claim 17 wherein the charge control
2   voltage generation circuit topology further comprises a current source
3   connected between one of the plurality of resistors and a power supply
4   voltage.

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1　　　　20.　The imaging system of either of claims 18 or 19 wherein the
2　current source comprises a variable current source.

1　　　　21.　The imaging system of claim 1 wherein the charge control
2　voltage generation circuit topology comprises a digital register for each
3　charge control voltage in the plurality of voltages.

1　　　　22.　The imaging system of claim 1 wherein the charge control
2　voltage generation circuit topology comprises a sample-and-hold amplifier
3　for each charge control voltage in the plurality of voltages.

1　　　　23.　The imaging system of claim 1 wherein each charge control
2　voltage comprises a substantially constant voltage level, the plurality of
3　voltages together comprising a stepped sequence of voltage levels.

1　　　　24.　The imaging system of claim 23 wherein the stepped sequence
2　of constant voltages comprises a sequence of decreasing voltage levels.

1　　　　25.　The imaging system of claim 1 wherein the plurality of charge
2　control voltages together comprise a substantially continuously-changing
3　voltage level.

1　　　　26.　The imaging system of claim 1 wherein the pixel transfer
2　function corresponding to the plurality of charge control voltages comprises
3　a nonlinear transfer function.

1　　　　27.　The imaging system of claim 1 wherein the switch circuit
2　comprises a plurality of MOS transistor switches.

1   28.   The imaging system of claim 1 wherein the switch circuit

2   connection to the pixel array is configured to apply the charge control

3   voltages to rows of the pixel array sequentially.

1   29.   An imaging system comprising:

2   a MOS pixel array including rows of pixels, each pixel including a

3   light detecting element, a reset node connected to the light detecting

4   element for controlling dissipation of photogenerated charge produced by

5   the light detecting element, and a sense node connected to the light

6   detecting element for measuring photogenerated charge produced by the

7   light detecting element;

8   a charge control voltage generation circuit including a circuit topology

9   for producing a plurality of charge control voltages selected to control

10   dissipation of photogenerated charge produced by the light detecting

11   element, in accordance with a corresponding pixel transfer function; and

12   a switch circuit connected to the voltage generation circuit and

13   connected to the pixel array to apply voltages produced by the charge

14   control voltage generation circuit to reset nodes of pixels, application by the

15   switch circuit of each of the charge control voltages to the reset nodes of

16   each of the pixels in the pixel array being characterized by a voltage

17   application settling time, t_s, that is less than about a specified duration of

18   each control voltage in the plurality of control voltages.

1   30.   An imaging system comprising:

2   a MOS pixel array having a number, r, of rows of pixels, each pixel

3   including a light detecting element, a reset node connected to the light

4   detecting element for controlling dissipation of photogenerated charge

5   produced by the light detecting element, and a sense node connected to the

6   light detecting element for measuring photogenerated charge produced by

7   the light detecting element;

8   a charge control voltage generation circuit including a circuit topology

9   comprising a series connection of a plurality of resistors and a current

10 source between a power supply voltage and electrical ground, for producing

11 a plurality of charge control voltages selected to control dissipation of

12 photogenerated charge produced by the light detecting element, in

13 accordance with a corresponding pixel transfer function; and

14   a switch circuit connected to the voltage generation circuit and

15 connected to the pixel array to apply voltages produced by the charge

16 control voltage generation circuit to reset nodes of pixels, application by the

17 switch circuit of each of the charge control voltages to a row of pixel reset

18 nodes being characterized by a voltage application settling time, t_s, that is

19 less than about $1/Nrf$, where N is an integer and f is imager frame rate.

1   31.   A charge control voltage generation circuit for producing a

2 plurality of charge control voltages selected to control dissipation of

3 photogenerated charge, produced by a pixel of a MOS pixel array, in

4 accordance with a corresponding pixel transfer function, the voltage

5 generation circuit including a circuit topology that is characterized by a

6 Thevenin resistance, R_{th}, that is less than about $1/NrfC$, where N is an

7 integer, r is a number of rows of MOS pixels in the pixel array, f is pixel

8 array frame rate, and C is an effective capacitance of the pixel array.

1   32.   The charge control voltage generation circuit of claim 31

2 wherein at least one of the produced voltages comprises a variable voltage.

1   33.   The charge control voltage generation circuit of claim 31

2 wherein the charge control voltage generation circuit topology comprises a

3 plurality of resistors and a voltage source.

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1   34.   The charge control voltage generation circuit of claim 31
2   wherein the charge control voltage generation circuit topology comprises a
3   plurality of resistors and a current source.

1   35.   The charge control voltage generation circuit of claim 34
2   wherein the current source comprises a variable current source.

1   36.   The charge control voltage generation circuit of claim 34
2   wherein the current source comprises a transistor current source.

1   37.   The charge control voltage generation circuit of claim 31
2   wherein the charge control voltage generation circuit topology comprises a
3   series connection of a plurality of resistors between two voltages.

1   38.   The charge control voltage generation circuit of claim 37
2   wherein the two voltages of the charge control voltage generation circuit
3   topology comprise a power supply voltage and electrical ground.

1   39.   The charge control voltage generation circuit of claim 38
2   wherein the charge control voltage generation circuit topology further
3   comprises a current source connected between one of the plurality of
4   resistors and electrical ground.

1   40.   The charge control voltage generation circuit of claim 38
2   wherein the charge control voltage generation circuit topology further
3   comprises a current source connected between one of the plurality of
4   resistors and a power supply voltage.

1   41.   The charge control voltage generation circuit of either of claims
2   39 or 40 wherein the current source comprises a variable current source.

1   42.   The charge control voltage generation circuit of claim 31
2   wherein the integer N is at least 2.

1   43.   The charge control voltage generation circuit of claim 31
2   wherein each charge control voltage comprises a substantially constant
3   voltage level, the plurality of voltages together comprising a stepped
4   sequence of voltage levels.

1   44.   The charge control voltage generation circuit of claim 43
2   wherein the stepped sequence of constant voltages comprises a sequence of
3   decreasing voltage levels.

1   45.   The charge control voltage generation circuit of claim 31
2   wherein the plurality of charge control voltages together comprise a
3   substantially continuously-changing voltage level.

1   46.   The charge control voltage generation circuit of claim 31
2   wherein the pixel transfer function corresponding to the plurality of charge
3   control voltages comprises a nonlinear transfer function

1   47.   The charge control voltage generation circuit of claim 31
2   wherein the charge control voltage generation circuit topology is
3   monolithically integrated with the MOS pixel array.

1   48.   A charge control voltage generation circuit for producing a
2   plurality of charge control voltages selected to control dissipation of
3   photogenerated charge, produced by a pixel of a MOS pixel array, in
4   accordance with a corresponding pixel transfer function, the voltage
5   generation circuit including a circuit topology that is characterized by a

6   settling time, $t_s = R_{th}C$, where R_{th} is the Thevenin resistance of the circuit

7   topology and C is an effective capacitance of the pixel array, the settling

8   time being less than about a specified duration of each control voltage in the

9   plurality of charge control voltages.

1   49.   A method for controlling photogenerated charge dissipation in

2   a pixel of a MOS imager pixel array to produce a selected pixel transfer

3   function, the pixel array having a number, r, of pixel rows and operating at

4   a frame rate, f, the method comprising the steps of:

5   generating a plurality of charge control voltages selected to control

6   dissipation of photogenerated charge produced by the pixel in accordance

7   with a corresponding pixel transfer function; and

8   applying the generated charge control voltages to a reset node of the

9   pixel during a pixel exposure period to control dissipation of photogenerated

10   charge produced by the pixel, application of each of the charge control

11   voltages being characterized by a voltage application settling time, t_s, that is

12   less than about $1/Nrf$, where N is an integer.

1   50.   The method of claim 49 wherein the charge control voltages are

2   generated by a charge control voltage circuit that is monolithically

3   integrated with the MOS imager pixel array.

1   51.   The method of claim 49 wherein the charge control voltage

2   application settling time, t_s, is given as $t_s = R_{th}C$, where R_{th} is an effective

3   Thevenin resistance of a charge control voltage generation circuit from

4   which the charge control voltages are generated, and C is the effective

5   capacitance of the imager pixel array.

1   52.   The method of claim 49 wherein the integer N of the settling

2   time is at least 2.

1   53.   The method of claim 49 wherein each charge control voltage

2 comprises a substantially constant voltage level, the plurality of voltages

3 together comprising a stepped sequence of voltage levels.

1   54.   The method of claim 53 wherein the stepped sequence of

2 constant voltages comprises a sequence of decreasing voltage levels.

1   55.   The method of claim 49 wherein the plurality of charge control

2 voltages together comprise a substantially continuously-changing voltage

3 level.

1   56.   A method for controlling photogenerated charge dissipation in

2 a pixel of a MOS imager pixel array to produce a selected pixel transfer

3 function, the pixel array including rows of pixels and operating at a frame

4 rate, f, the method comprising the steps of:

5   generating a plurality of charge control voltages selected to control

6 dissipation of photogenerated charge produced by the pixel in accordance

7 with a corresponding pixel transfer function; and

8   applying the generated charge control voltages to a reset node of the

9 pixel during a pixel exposure period to control dissipation of photogenerated

10 charge produced by the pixel, application of each of the charge control

11 voltages being characterized by a voltage application settling time, t_s, that is

12 less than about a specified duration of each control voltage in the plurality

13 of control voltages.
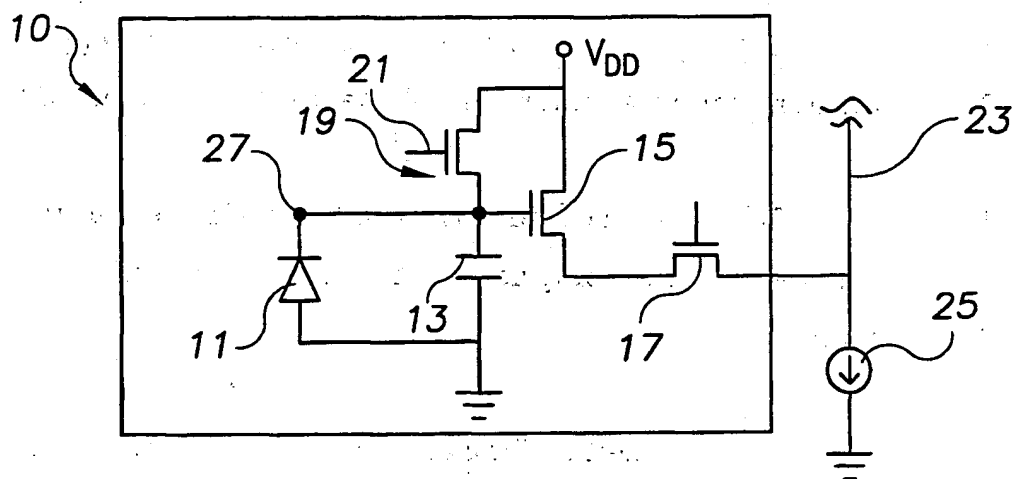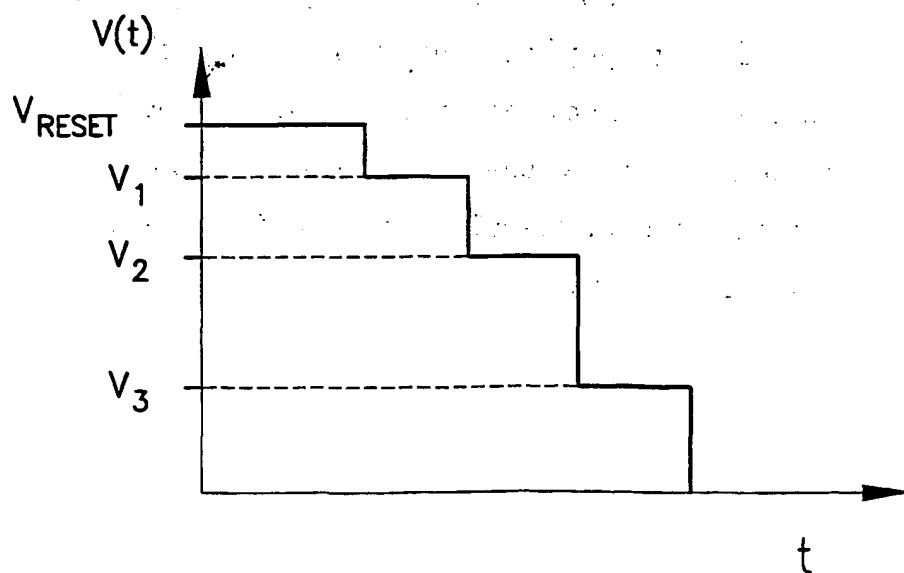
FIG.1

FIG.2

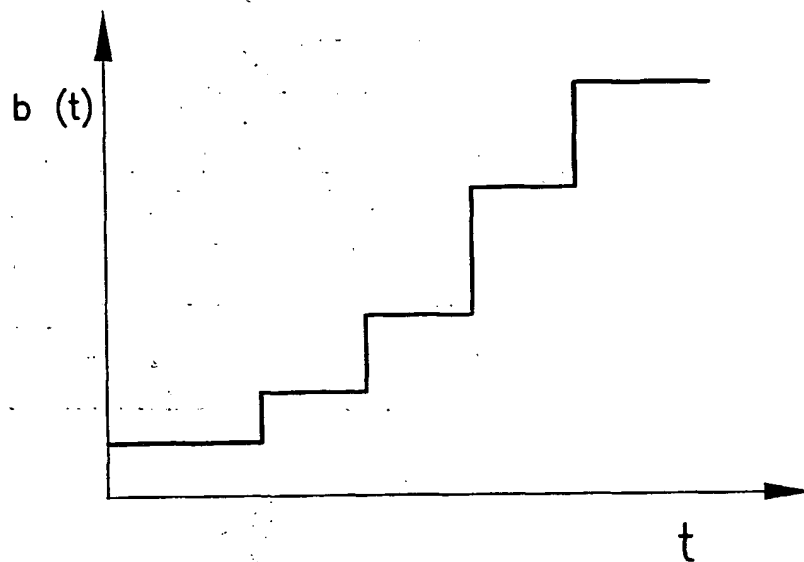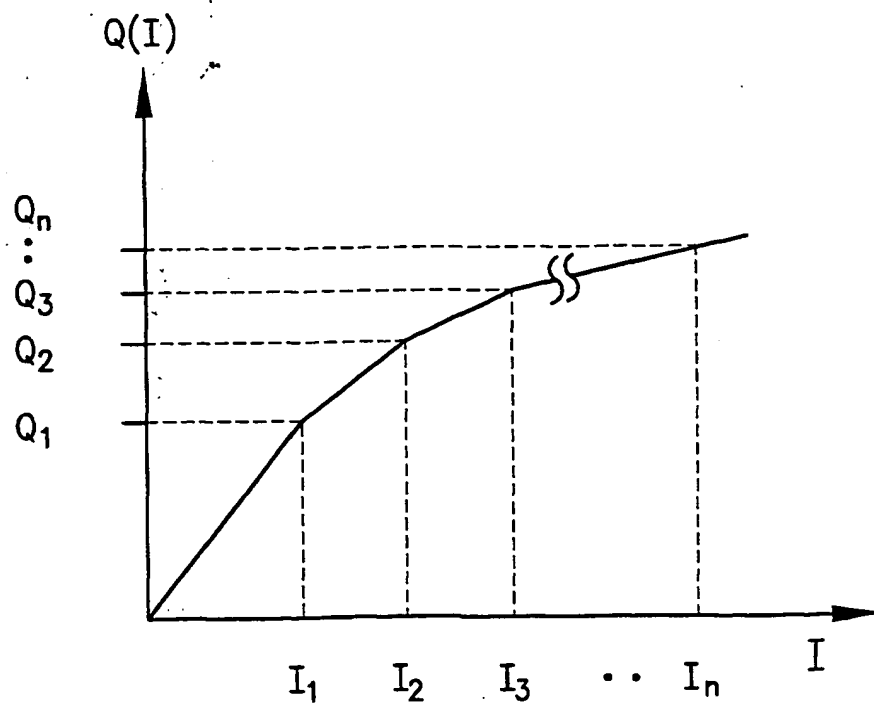# FIG.3

FIG.4

FIG.5

FIG.6A

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FIG.6B

FIG.6C

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FIG.7

FIG.8

FIG.9

V_TOP ... I ... V_RESET ... R_1 ... V_2 ... R_2 ... V_1 ... V_n ... R_{n+1} ... V_BOTTOM

FIG.10

V_DD ... R_1 ... V_1 ... R_2 ... V_2 ... R_3 ... V_3 ... V_n ... R_{n+1} ... V_S
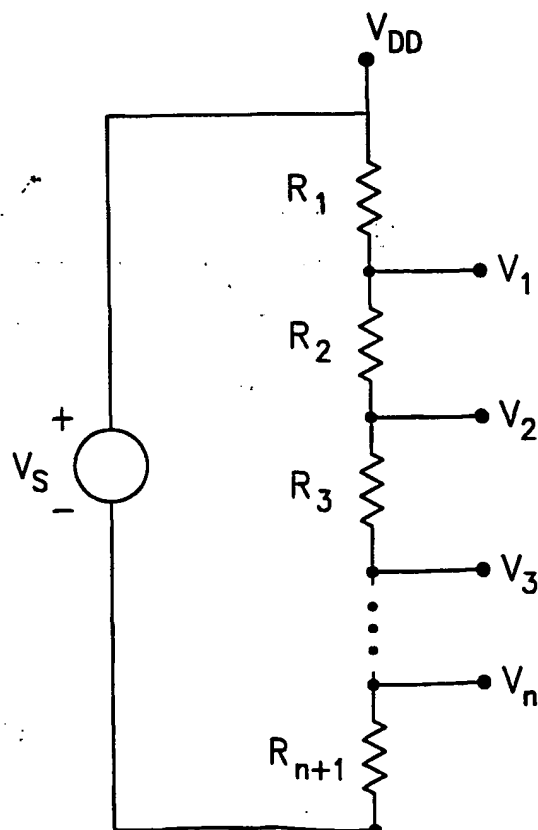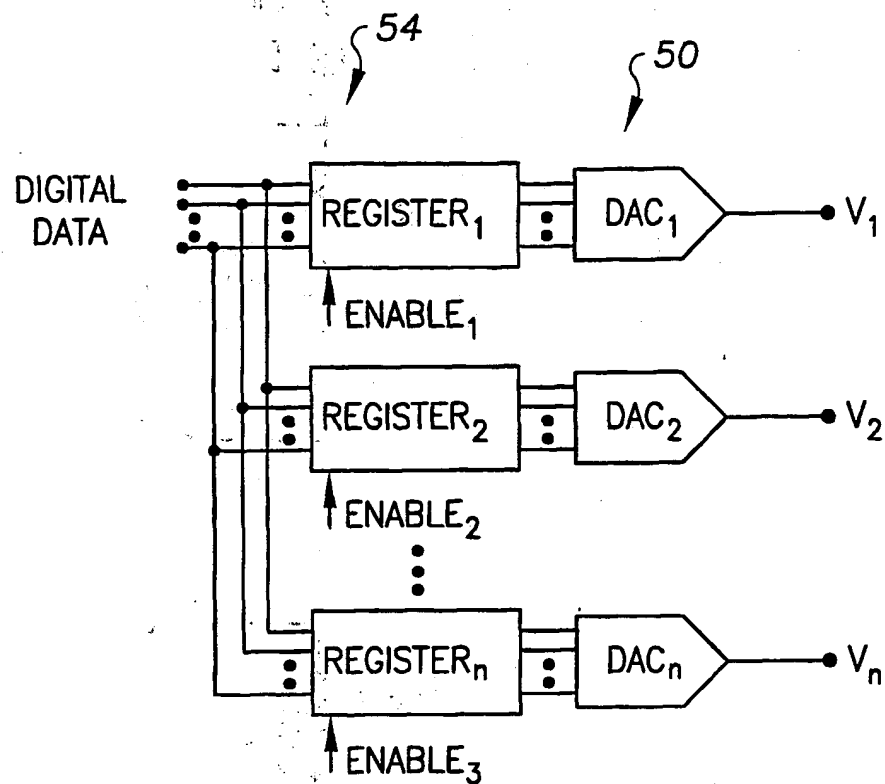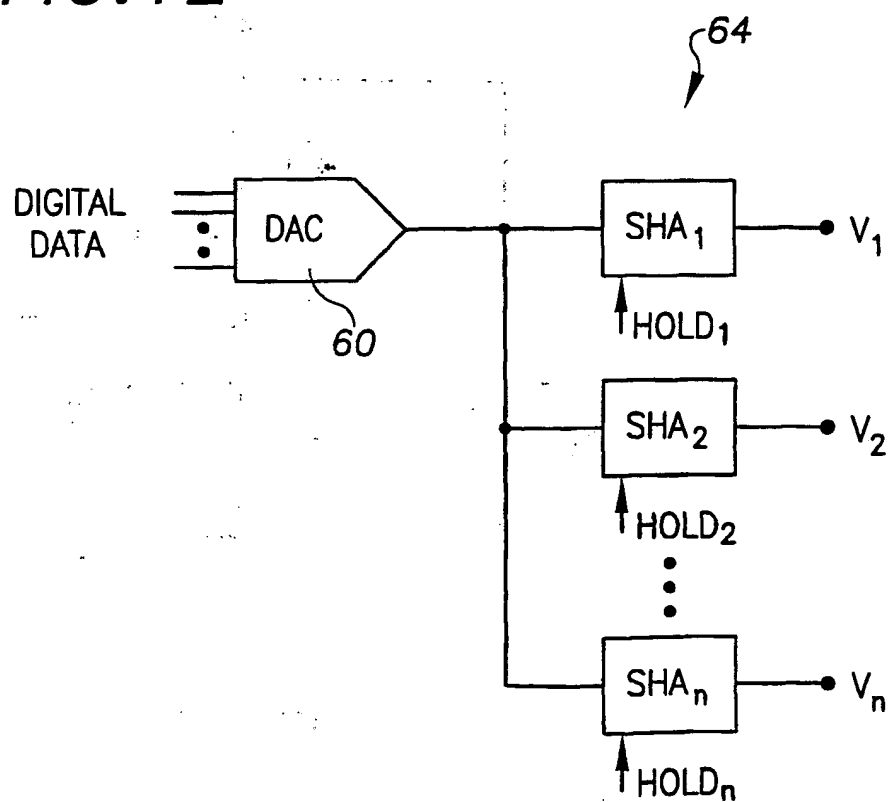
FIG.11

FIG.12

INTERNATIONAL SEARCH REPORT
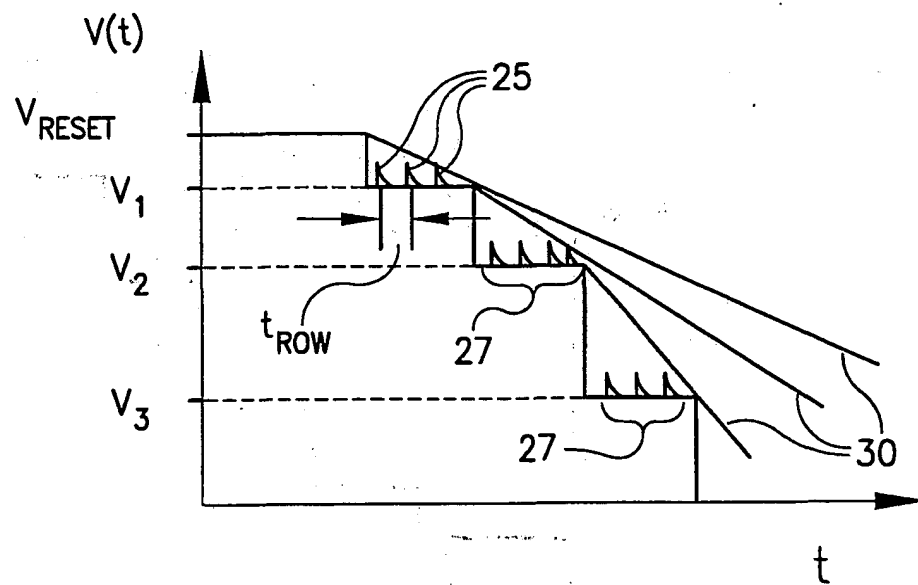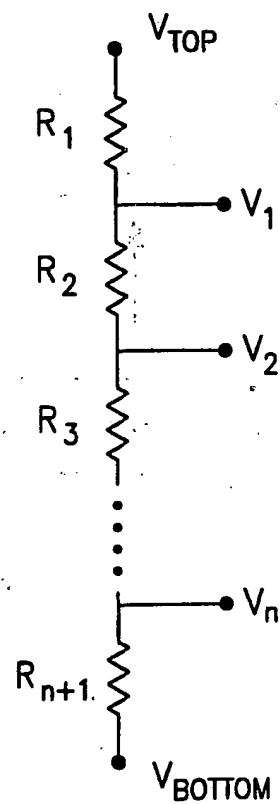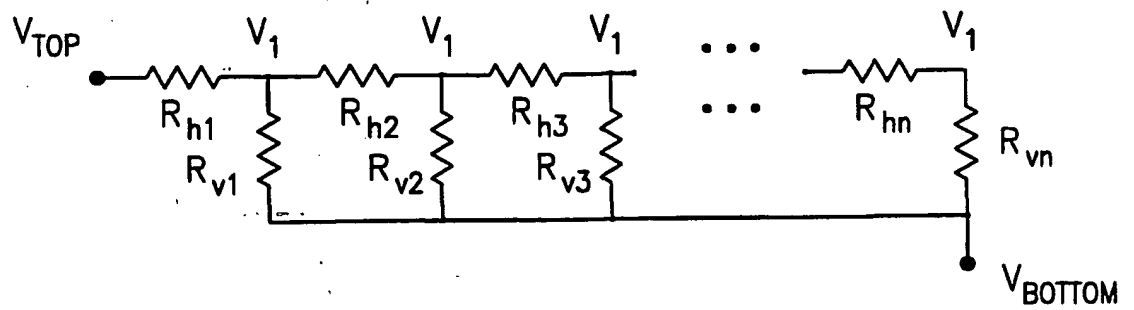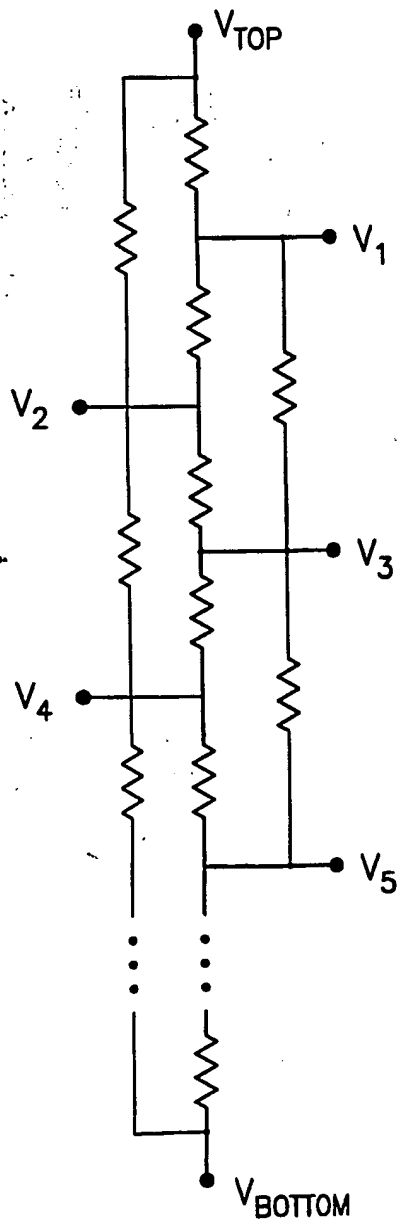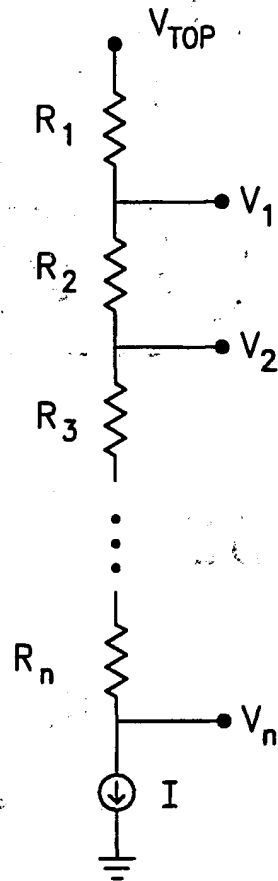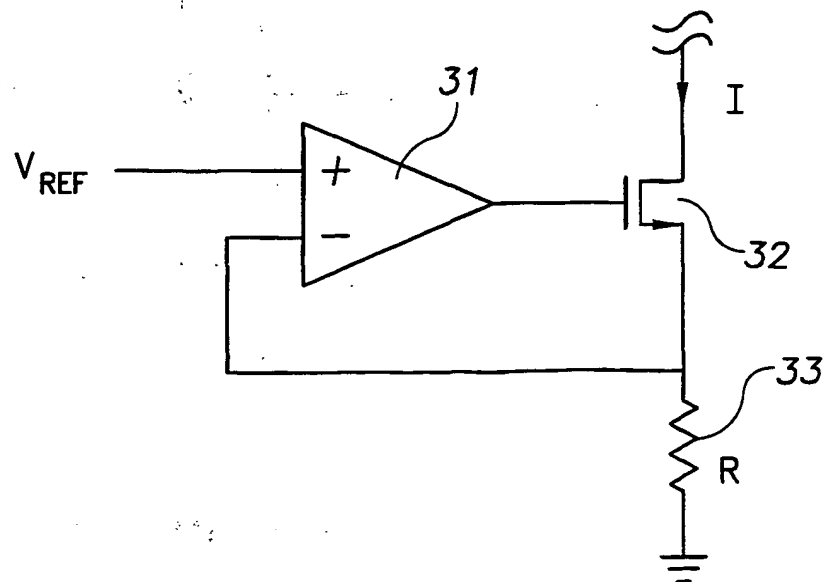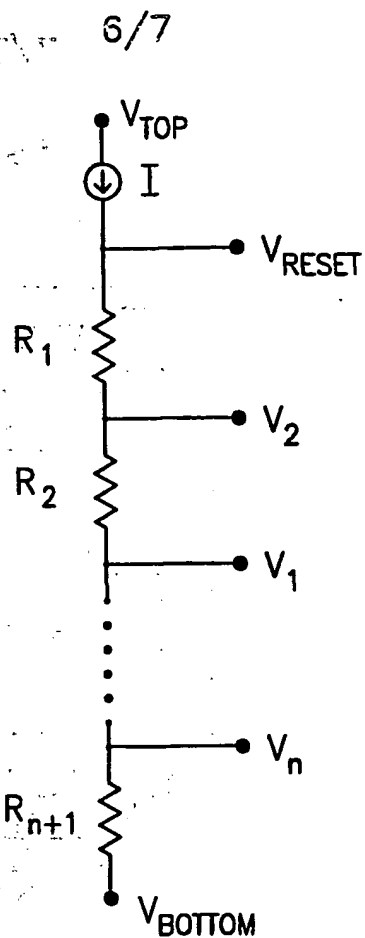
A. CLASSIFICATION OF SUBJECT MATTER

IPC 7   H04N3/15

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7   H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 99 66560 A (FOVEON INC) 23 December 1999 (1999-12-23) page 2, line 16 – line 25 page 15, line 29 –page 16, line 8; figure 8	1,29-31, 48,49,56
A	GB 2 330 905 A (HEWLETT PACKARD CO) 5 May 1999 (1999-05-05) page 8, line 16 –page 9, line 3; figure 9	1,29-31, 48,49,56
A	WO 99 49571 A (COLLINS STEVEN ;SECR DEFENCE (GB); MARSHALL GILLIAN FIONA (GB)) 30 September 1999 (1999-09-30) page 10, line 4 – line 10	1,29-31, 48,49,56

☐ Further documents are listed in the continuation of box C.   ☒ Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
2 October 2001	09/10/2001

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Bequet, T |

Form PCT/ISA/210 (second sheet) (July 1992)

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